Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A14**
2. **IO4**
3. **NC**
4. **IO5**
5. **NC**
6. **NC**
7. **VDD**
8. **VDD**
9. **VDD**
10. **VSS**
11. **VSS**
12. **NC**
13. **VSS**
14. **IO6**
15. **NC**
16. **IO7**
17. **NC**
18. **/OE**
19. **NC**
20. **NC**
21. **NC**
22. **A15**
23. **A16**
24. **A17**
25. **A18**
26. **A0**
27. **NC**
28. **NC**
29. **A1**
30. **A2**
31. **A3**
32. **A4**
33. **/CS**
34. **IO0**
35. **NC**
36. **IO1**
37. **NC**
38. **NC**
39. **VDD**
40. **VDD**
41. **VDD**
42. **VSS**
43. **VSS**
44. **NC**
45. **VSS**

**46 IO2**

**47 NC**

**48 IO3**

**49 NC**

**50 /WE**

**51 A5**

**52 NC**

**53 A6**

**54 A7**

**55 A8**

**56 A9**

**57 NC**

**58 NC**

**59 NC**

**60 A10**

**61 A11**

**62 A12**

**63 NC**

**64 A13**

**1**

**2**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**12**

**13**

**14**

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**18**

**19**

**64 63 62 61 60 59 58 57 56 55 54 53 52 51**

**20 21 22 23 24 25 26 27 28 29 30 31 32**

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**LOGO**

**ISSI**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0025 X .0025”**

**APPROVED BY: DK DIE SIZE .143” X .181” DATE: 5/24/22**

**MFG: ISSI THICKNESS .012” P/N: IS64C5128AL**

**DG 10.1.2, Rev B, 7/1**Rev B, 7/1